Implementation of AHB-Based Communication Interface Integrating DMA and UART for Efficient Data Transfer

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ABSTRACT
UART is a transmission device & high speed soc is AHB bus. in this paper high speed components are interfaced to low speed components by using AHB bus.AHB bus is used to transmit data from DMA to memory& high speed components are connected by using this AHB bus. Compared to other system buses performance & processing time of soc is improved by using AHB bus. In serial communication UART controller plays a major role. Transmission of digital information through single wire is much more cost effective than transmitting through multiple wires. At the end of every link UART converts transmitted information between sequential & parallel form. For this purpose UART has shift registers.

There are five main modules. Those are UART transmitter, UART receiver, DMA (direct memory access) master read controller, DMA master write controller, AHB (advanced high performance bus).

KEYWORDS: UART,DMA,AHB, Memory, communucation.

INTRODUCTION
In serial communication UART controller plays a major role. UART transmitter transmits individual bits in sequential fashion by taking bytes of data. At destination UART receiver reassembles the transmitted individual bits into bytes. Transmission of digital information through single wire is much more cost effective than transmitting through multiple wires. At the end of every link UART converts transmitted information between sequential & parallel form. UART s are generally used along with some communication standards like EIA (electronic industrial association) & RS-232.

DMA (direct memory access) is used to access memory directly without accessing CPU. All data transfer operations are controlled by DMA so that CPU can handle other things without any disturbance. By using DMA the occupancy time of CPU is reduced with increase in overall system performance.DMA controllers are used to control transfer of data to and from peripheral devices like UART.

UART BLOCK DIAGRAM
In Subsystem of computer UART is a key component. Data format of UART consists of 11bits.these are active low start bit, data bits(8),parity bit & high stop bit. Active low start bit indicates the receiving UART that it is sending a sequence then receiving UART receives next 8 bits followed by parity bit may be either even or odd parity. Then the high stop Bit indicates the end of the block.

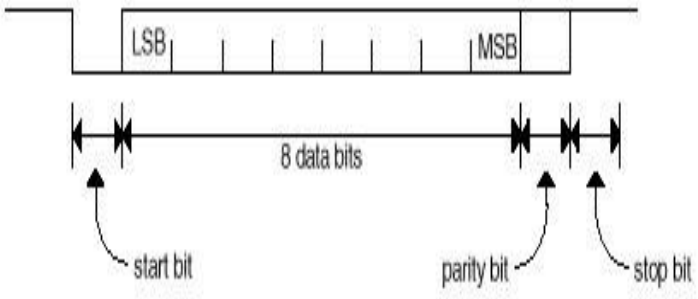


Fig1.Data format of UART

UART TRANSMITTER
Tx enable is high then it enables this block to transmit the data. if it is low then the transmitter state machine is in IDLE state. To enable parity state 8bit data is used.RST pin used to reset the block. when parity phase is set to

0 or 1 then the transmit logic inserts the required parity bit into outing TXD bit stream. TX-FREE is output signal of transmitter when it is high it indicates transmitter is free 7 ready

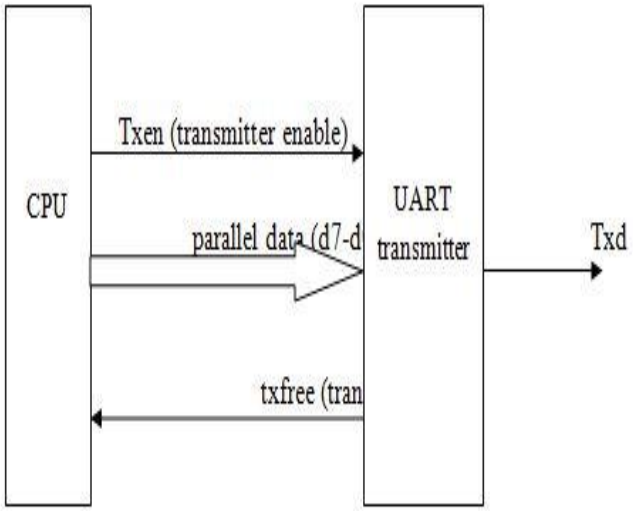


Fig2. UART transmitter

UART RECIVER

The receiving signal sequence is shown in above fig:. data is received bit by bit by using the serial reception line rxd. start and stop bits are removed when the receiver starts its reception and data is placed in internal buffers. Following figure shows the UART receiver.

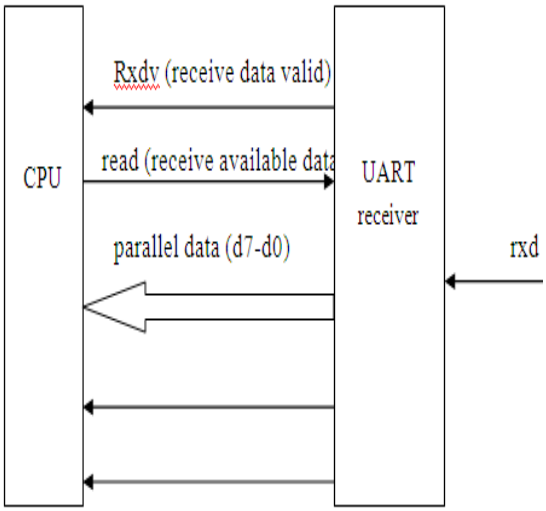


Fig3.UART receiver

DMA (DIRECT MEMORY ACCESS)

DMA to the memory access controller is a peripheral device to the computer. It performs sequence of transfer on behalf of CPU. It also moves data from one memory location to other on specified stimulus. but it is limited in flexibility.DMA controller transfers data to & from peripheral devices such as UART. when byte is received UART generates DMA request then DMA requests for bus grant when bus is granted it reads data from UART address followed by a write to memory.

DMA BLOCK DIAGRAM

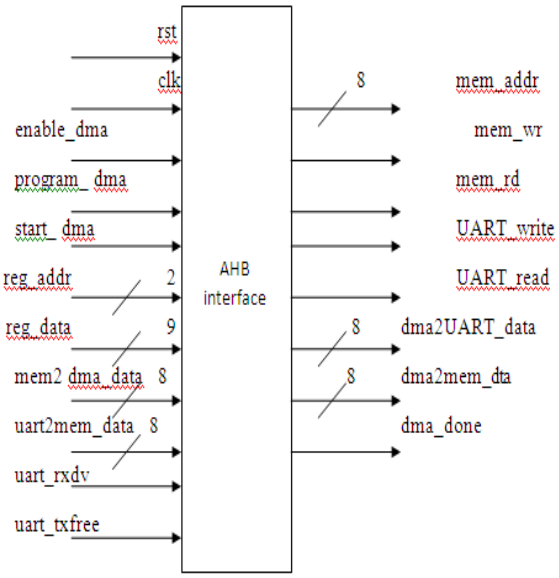


Fig4.DMA block diagram

Figure shows different inputs & outputs of the DMA from & to UART & memory .CPU programs DMA so that it knows source address & destination address & transfer count.cpu programs DMA registers. If the input signals pgm_dma is high. Reg_addr is 2 input signals, depending on these two input signal CPU assigns different things to DMA. Source addresses is assigned if it is 00,destination address is assigned if it is 01,transferlength is assigned if it is 10.source address &destination address is hold by 9 bit wide input Line reg---data.Mem2dma---data and uart2dma---data are also two 8 bit data lines, One is from memory to DMA. Destination other is from UART to DMA. uart---rxdv &uart2dma---data are asserted from receiver to DMA. Received data from receiver is read by asserting uart-_read high with uart_rxdv is set as high read, write & addresses to memory are provided to DMA by output signals mem_wr, mem_addr. DMA reads data from memory through the line mem2dma---data. Transmitter indicates its readiness by using the input signal uart_txfree.at last dma_done shows the completion of DMA operation.

DMA STATE MACHINE

When the processor sends that through serial port, Firstly, it's necessary to make configuration to the UART sent controller and the Master Read type DMA controller through the register file with the interface of Avalon-MM slave to set the serial port, the number of bytes of the data to be sent and the address of the data stored in the memory.FIG shows DMA state transition diagram.

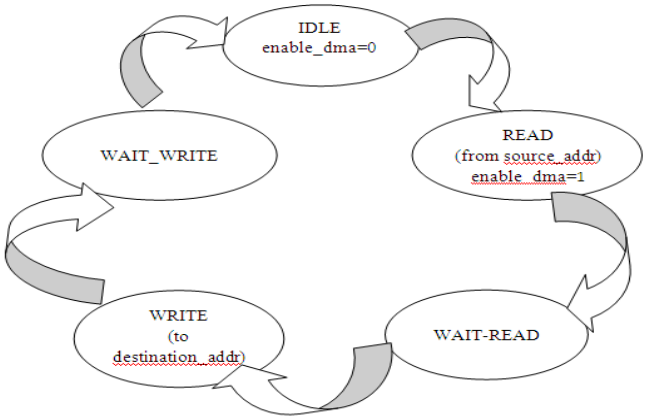


Fig5. State machine of DMA

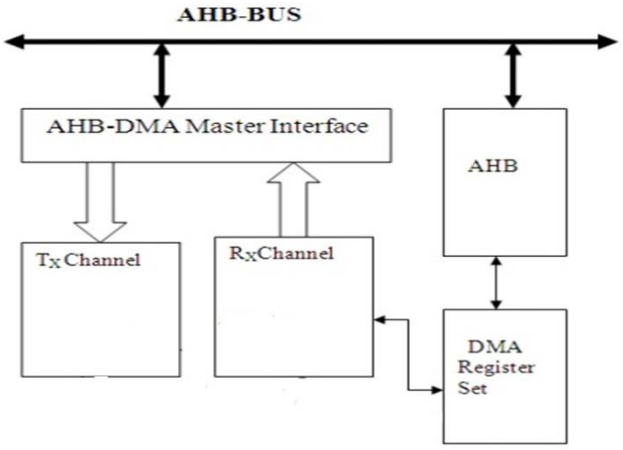
Secondly, write the data to be sent the specified location in the memory and then start the Master reader type DMA controller, thus the data stored in the memory is sent out one by one through the UART sent controller. When all the data that you want to send has been sent, an interrupt will be generated in the processor to inform the processor that the transmission of serial data is completed, so as to start the next data transmission. The whole process of data sent is managed by the Master Read type DMA controller; processor will concentrate on other things and not to be disturbed, so that the utilization ratio of CPU increases greatly. When the processor need to receive data through serial ports, firstly, it's necessary to fulfill the configuration on the UART receive controller and a Master Write type of DMA controller through the register file sets baud rate of the serial port, the number of bytes of data which will be received and the base address of the data stored in the memory.

Start the Master Write type of DMA controller, so that the data received through the UART controller can be stored in the specified location in the memory one after the one, when all the data is received, then an interrupt will be generated in the processor to inform the processor that the transmission of serial data is completed, so as to read the data which is received from the memory for processing and started the next data transmission. Since the Master Write type of DMA controller manages the whole process of data reception, processor can concentrate on other things and not be disturbed, thus the utilization ratio of CPU increased substantially.

In the present thesis DMA with only one channel is implemented. But in general there may be more than one channel in DMA controller. Each channel will have a separate master and slave. Each channel works independently on other channels.

The CPU handles all these channels .before transferring data CPU programs the DMA to let it know source and destination. So that the DMA knows source address and destination address.

BLOCK DIAGRAM OF DMA with AHB and UART



ADVANCED HIGH PERFORMANCE BUS (AHB)

Single layer AHB

AHB supports single data access and various types of burst accesses. Each transfer is defined by an address. A data phase where the address phase of one transfer occurs during the data phase of the previous transfer. AHB is traditional bus architecture between multiple masters with arbitration. The protocol supports advanced features such as SPLIT and RETRIES signaling in cases where a slave is not able to respond immediately. The masters who have been granted the bus will back off until then other masters will get a turn.

Multilayer AHB

Instead of a complex multiplexing scheme, a AHB bus architecture with M masters and S slaves is structured as M * 1:S multiplexers plus S * M:1 slave multiplexers all connected to separate arbitration and decoding logic.
Multiple masters can talk to multiple slaves concurrently, until no two masters don't try to access the same slave at same time. Think of a DMA controller which is moving data from receiver into memory region, while the processor continues to execute code in a different memory. The arbitration and complexity of protocol moves into the fabric. The interface implementation becomes simpler as a number of unneeded signals can be removed along with their associated protocol.

RESULTS

The below one shows the simulation result of DMA with AHB and UART peripheral.

Fig 6: Simulation Result of DMA with AHB and UART

With simulation results, synthesis results are also provided below.

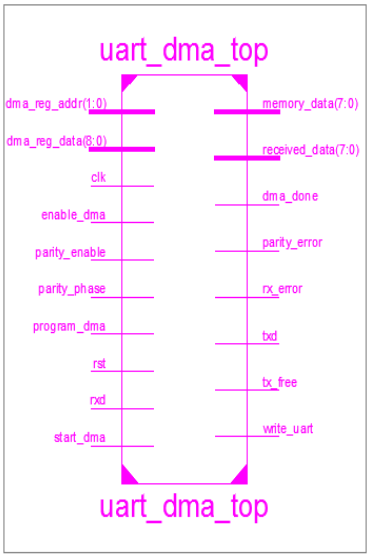


Fig 7: Top module

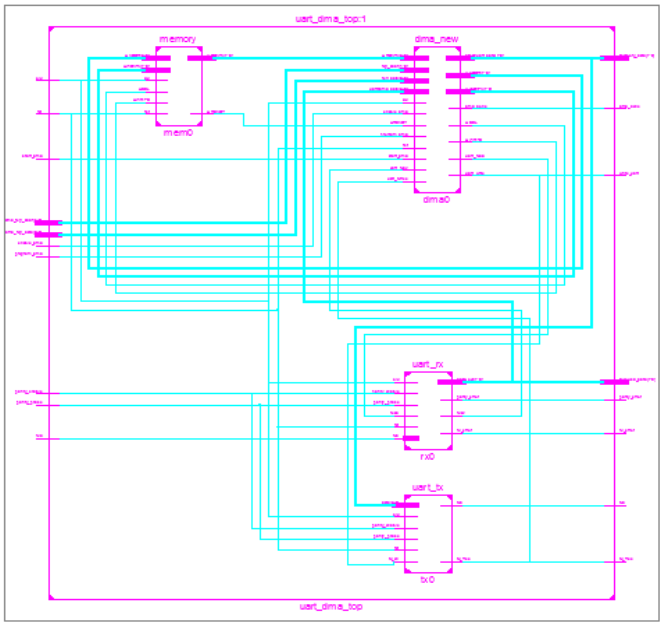


Fig 8: RTL schematic

CONCLUSION & SCOPE OF FUTURE DEVELOPMENT

Built-In-Self-Test (BIST) is one of the most popular test techniques. A BIST Universal Asynchronous Receive /Transmit (UART) with DMA has the objectives of firstly to satisfy specified testability requirements, and secondly to highest performance implementation can be generate with lowest-cost. UART has been an important input/output tool for decades and is still widely used.

BIST techniques are becoming more common in industry. The additional BIST circuit increases then the hardware overhead increases the design time and performance degradation is often cited as the reason for the limited use of BIST.

The technique can provide shorter test time compared to an externally applied test and allows using of low-cost test equipment at all the stages of production. At the implementation phase BIST technique is incorporated into UART design before synthesizing the overall design by reconfiguring the previous existing design to match requirements of testability. The UART is targeted at broadband modem, base station, cell phone, and PDA designs.

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